UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,544	04/12/2004	Peter Pfann	P2003,0235	1800

29393 7590 01/11/2007

ESCHWEILER & ASSOCIATES, LLC
NATIONAL CITY BANK BUILDING
629 EUCLID AVE., SUITE 1000
CLEVELAND, OH 44114

EXAMINER	
JACKSON, BLANE J	
ART UNIT	PAPER NUMBER
2618	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/822,544	PFANN ET AL.	
	Examiner	Art Unit	
	Blane J. Jackson	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement filed 10 November 2005 and 19 July 2004 have been received and placed of record in the file.

Response to Arguments

Applicant's arguments, see the Remarks, filed 04 October 2006, with respect to the rejection(s) of claim(s) 1-23 under Vu et al., Auvray and Horton et al. have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Boos, Auvray and Bellaouar et al.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boos (US 7,103,343) in view of Auvray (US 5,953,641) and Bellaouar et al. (US 2005/0070325).

As to claim 1, Boos teaches an integrated transceiver circuit (figure 2, a transceiver operating in the GSM and UMTS standard with high integration density, column 1, lines 15-43) comprising:

A reception path including a mixer unit for demodulating a received signal and also including an analog/digital converter unit connected downstream from the mixer unit (figures 1 and 2, column 4, lines 10-24), and

A first voltage controlled oscillator (figure 2, column 5, line 62 to column 6, line 2, VCO of PLL1 which is the local oscillator for the receive path).

Boos teaches a *first amplifier* connected between the first voltage controlled oscillator and the mixer unit, figure 2, amplifier (V) at the output of PLL1, but does not teach a first frequency divider connected between the first voltage controlled oscillator and the mixer unit.

Auvray teaches a dual mode radio communication transceiver circuit comprising controlled switches to select whether the synthesized local oscillator signal is connected to the mixer unit or frequency divided and then applied to the mixer unit in accordance to the user selected frequency band or mode of communication, figure 1, column 4, lines 33-48. Auvray further discloses additional changes to the synthesized local oscillator frequency by an operation such as division, multiplication, addition or subtraction to obtain the frequencies of a plurality of other frequency bands to provide a multimode terminal, column 4, lines 52-65.

Since Boos discusses the desirability of selected circuits to provide a dual mode cellular telephone, column 3, lines 31-40, it would have been obvious to one of ordinary

skill in the art at the time of the invention to modify the local oscillator circuits of Boos in accordance to the switched frequency divider circuits of Auvray to further provision a multimode cellular telephone.

Boos of Boos modified teaches a frequency multiplier or divider may or may not be used connected between the *reference oscillator* and the analog/digital converter unit for obtaining a sampling frequency for use by the analog/digital converter unit, column 5, lines 31-40, but does not teach a second frequency divider connected between the first voltage controlled oscillator and the analog/digital converter unit.

Bellaouar teaches a direct conversion receiver comprising an oscillator or phase lock loop (PLL) (66) coupled to the mixer unit for frequency downconversion and also coupled to a frequency divider (55) which outputs a sampling frequency to the quadrature analog to digital converters (ADC) (58, 60), figure 2a, paragraphs 0032 and 0057. Bellaouar further discloses the output of the frequency divider (55) is coupled to and provides timing signals for other elements of the receiver where the DSP (62) controls the PLL (66) and the frequency divider to set the operating frequency of the receiver, paragraph 0057.

Since Boos teaches a frequency multiplier or divider may be used to derive the correct timing signal to the ADC's, It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the ADC sample rate derivation of Boos modified in accordance with the alternative configuration of Bellaouar to generate a receiver timing frequency compatible with the selected operating frequency band.

As to claim 2, Boos teaches the integrated transceiver circuit of claim 1 further including a transmission path having a modulator for modulating a signal to be transmitted, a second voltage controlled oscillator (figure 2, VCO of PLL2 as the local oscillator for the transmit path). Boos teaches a *second amplifier (V)* connected between the first voltage controlled oscillator and the mixer unit, figure 2, amplifier (V) at the output of PLL2, but does not teach a third frequency divider connected between the second voltage controlled oscillator and the mixer unit.

Auvray teaches a transceiver comprising a single PLL (SYN) and single frequency divider (DIV) connected between the frequency synthesizer (SYN) or VCO and demodulation/ modulation circuits for selective use by the reception and transmission path, figure 1, column 4, lines 33-48. Auvray further discloses additional changes to the synthesized local oscillator frequency by an operation such as division, multiplication, addition or subtraction to obtain the frequencies of a plurality of other frequency bands to provide a multimode terminal, column 4, lines 52-65.

Since Auvray teaches the idea of selective use of frequency division to the reception and transmit signal paths for the purpose of multimode operation, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the dual VCO system of Boos of Boos modified to include a frequency divider as taught by Auvray but for both VCO circuits as represented in the PLL1 and PLL2 output drive amplifiers as taught by Boos for multimode operation of the transceiver.

As to claim 3 with respect to claim 2, Boos teaches the transmission path includes a digital/analog converter unit connected upstream of the modulator and including a fourth frequency divider connected between *the reference frequency oscillator* and the digital/analog converter unit for obtaining sampling frequency for use by the digital/analog converter unit (figures 1 and 2, option multiplier (MP2) shown, column 4, lines 54-67. Boos further teaches a frequency multiplier or divider may be used to derive the correct timing signal to the ADC's column 5, lines 32-40 but does not teach a fourth frequency divider connected between the second voltage controlled oscillator and the digital/analog converter.

Bellaouar teaches a direct conversion receiver comprising an oscillator or phase lock loop (PLL) (66) coupled to the mixer unit for frequency downconversion and also coupled to a frequency divider (55) which outputs a sampling frequency to the quadrature analog to digital converters (ADC) (58, 60), figure 2a, paragraphs 0032 and 0057. Bellaouar further discloses the output of the frequency divider (55) is coupled to and provides timing signals for other elements of the receiver where the DSP (62) controls the PLL (66) and the frequency divider to set the operating frequency of the receiver, paragraph 0057.

Even though Bellaouar teaches the sampling frequency is derived for the receive path ADC, it would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the transmit path DAC sample rate derivation of Boos modified in accordance with the alternative approach of Bellaouar to generate a transmitter timing frequency compatible with the selected operating frequency band.

As to claims 4 and 17 with respect to claims 3 and 16, Boos teaches the integrated transceiver circuit including a reference frequency input for receiving an external reference frequency and a first phase locked loop connected between the reference frequency input and the first voltage controlled oscillator (figures 1 and 2, reference frequency (RG) coupled to PLL1 which comprises a VCO that outputs to drive the receive path mixer unit).

As to claim 5, Boos teaches the integrated transceiver circuit of claim 4 including a second phase locked loop connected between the reference frequency input and the second voltage controlled oscillator (figure 2, column 4, lines 54-67, frequency reference (RG) coupled to PLL2 comprising a voltage controlled oscillator (VCO)).

As to claims 6, 8, 10 and 14 with respect to claims 5, 8, 3 and 2, Boos is silent wherein the reception path includes a digital signal processing unit connected downstream from the analog/digital converter unit, the digital signal processing unit having an output which forms a digital output of the reception path. Bellaouar teaches a digital radio receive comprising a digital signal processor (62) to process the output of quadrature ADCs (58 and 60), figure 2a, paragraph 0004.

Since Boos teaches a modern digital radio, column 1, lines 23-36, it would have been obvious to one of ordinary skill in the art at the time of the invention to recognize the integrated transceiver of Boos would comprise a baseband DSP as taught by

Bellaouar since modern digital radios comprise integrated circuits that integrate DSP functionality and analog functionality on the same IC thereby allowing multiple communication standards to be supported on a single IC.

As to claims 7, 9, 11 and 15 with respect to claims 6, 8, 10 and 14, Bellaouar of Boos modified does not disclose as the reception path includes a digital/analog converter unit coupled to the output of the DSP unit, the digital/analog converter unit having an output which forms an analog output of the reception path.

Auvray teaches a multimode direct conversion digital transceiver where the reception path comprises a codec coupled to the demodulation stage which includes the digital to analog function to drive the voice speaker (HP) and analog to digital function for voice microphone (M) input, figure 1, column 2, lines 35-67.

It would have been obvious to one of ordinary skill in the art at the time of the invention to alternatively complete the reception circuit of Vu in the application of Auvray for voice communications.

As to claims 12 and 16 with respect to claims 3 and 2, Boos teaches the integrated transceiver circuit including a reference frequency input for receiving an external reference frequency, and a phase locked loop connected between the reference frequency input and the second voltage controlled oscillator (figures 1 and 2, reference frequency (RG) coupled to PLL2 which comprises a VCO for the transmit path mixer unit).

As to claim 13, Boos teaches the integrated transceiver circuit of claim 3 wherein the transmission path includes a low-pass filter unit connected between the digital/analog converter unit and the modulator (figure 2, filter (TP) between the DAC (DA) and modulator (M2, M2')).

As to claim 18 with respect to claim 2, Boos teaches the integrated transceiver circuit including a reference frequency input for receiving an external reference frequency and a first phase locked loop connected between the reference frequency input and the first voltage controlled oscillator (figures 1 and 2, reference frequency (RG) coupled to PLL1 which comprises a VCO that outputs to drive the receive path mixer unit).

As to claim 19, Boos teaches the integrated circuit of claim 2 wherein the modulator is an IQ modulator (figure 2, column 6, lines 3-16).

As to claim 20, Bellaouar of Boos modified teaches the integrated transceiver circuit of claim 1 wherein the analog/digital converter unit includes first and second analog/digital converters having respective sampling control inputs which are connected to an output of the second frequency divider (figure 2a, paragraph 0009, ADCs (58, 60) and frequency divider (55), the receiver integrated on a single integrated chip

As to claim 21, Boos teaches the integrated transceiver circuit of claim 1 wherein the reception path includes a low-pass filter unit connected between the mixer unit and the analog/digital converter unit (figure 2, filters (TP) in the receive path).

As to claim 22, Boos teaches the integrated transceiver circuit of claim 1 wherein the mixer unit is an IQ mixer (figure 2, column 5, lines 41-61).

As to claim 23 with respect to claim 1, Auvray of Boos modified teaches the fist and second frequency dividers are integer dividers (figure 1, divider (DIV), column 4, lines 42-48, in the example, a simple divide by two).

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Auvray (US 5,953,641) in view of Bellaouar et al. (US 2005/0070325).

As to claim 24, Auvray teaches a method for processing a signal comprising:

Obtaining a demodulation frequency for use by a mixer unit in a reception path of an integrated transceiver circuit with a first frequency divider connected between a first voltage controlled oscillator and the mixer circuit (figure 1, column 4, lines 33-65, synthesizer (SYN) comprises the VCO and is coupled directly to the receiver mixer unit or selectively switched through a frequency divider (DIV) to function as a dual mode cellular telephone),

Demodulating a received signal with the mixer unit and the obtained demodulation frequency (figure 1, column 2, lines 37-60, baseband demodulator (DEMOD)).

Auvray teaches a method for processing a signal but does not teach obtaining a sampling frequency for use by an analog to digital converter unit with a second frequency divider connected between the first voltage controlled oscillator and the analog to digital converter unit and performing a digitizing operation on the demodulated received signal with the analog to digital converter and the obtained sampling frequency.

Bellaouar teaches a direct conversion receiver comprising an oscillator or phase lock loop (PLL) (66) coupled to the mixer unit for frequency downconversion and also coupled to a frequency divider (55) which outputs a sampling frequency to the quadrature analog to digital converters (ADC) (58, 60), figure 2a, paragraphs 0032 and 0057. Bellaouar further discloses the output of the frequency divider (55) is coupled to and provides timing signals for other elements of the receiver where the DSP (62) controls the PLL (66) and the frequency divider to set the operating frequency of the receiver, paragraph 0057.

It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify Auvray the sample frequency derivation method of Bellaouar to generate a receiver timing frequency compatible with the selected operating frequency band.

Conclusion

The prior art made of record and not relied upon but considered pertinent to applicant's disclosure includes: Takaki et al. (US 2001/0014596), Tso et al. US 6,856,794), Claxton et al. (US 6,735,421) and Olsen (US 2003/0064699).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Blane J. Jackson whose telephone number is (571) 272-7890. The examiner can normally be reached on Monday through Friday, 9:00 AM-6:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Blane J. Jackson